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EXAMINER
FLOURNOY, HORACE L

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 06/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,772	SHIMADA ET AL.	
	Examiner	Art Unit	
	Horace L. Flournoy	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/25/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

As required by **M.P.E.P.** 609(c), the applicant's submission of the Information Disclosure Statement dated **05/25/2006** is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P.** 609(c), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-2 and 4-18 are rejected under 35 U.S.C. 103(a) as being obvious over Doing et al. (U.S. P.G. Publication Number 2003/0009648) in view of DeKoning et al. (U.S. Patent Number 6,216,199, hereafter referred to as DeKoning).

With respect to **independent claims 1, 16, and 18,**

Doing discloses:

> *"A storage to be connected to a network,* **[Doing teaches paragraph [0018], "...coupled to a network"]** *comprising: a host interface* **[Doing teaches in FIG. 1, elements 110, 114/115. The host is interpreted by the examiner as a workstation. Both workstation elements 114 and 115 interface to a network via elements 110 and 114/115]** *which is arranged to be connected to a host computer and the network* **[Doing teaches in paragraph [0018], "...coupled to a network"]** *and to receive file access from the host computer;* **[Doing teaches in paragraph [0055], "...instructions or data must be fetched or stored." See FIGs. 1 & 2]** *a plurality of disk drives* **[Doing teaches in FIG. 1, elements 111 and 112, "DASD"]** *and a control unit* **[Doing teaches on page 3, paragraph [0035]. Furthermore, FIG. 1, in its entirety is interpreted by the examiner, as a "control unit"]** *which translates data of the file access into block ~~access~~ data* **[Doing discloses in paragraphs [0037] and [0047]]** *and controls the plurality of disk drives on the basis of the block access* **[Doing teaches in**

paragraph [0035]] *the control unit including a first processor* **[Doing teaches in FIG. 1, element 101A]** *which translates the data of the file access into the block ~~access~~ data,* **[Doing discloses this limitation, e.g. in FIG. 5 (see all associated text within specification). Also see paragraph [0037]]** *a second processor* **[Doing discloses a "second processor" e.g. in FIG. 1 element 111: "Storage IOP"]** *which controls the plurality of disk drives on the basis of the block ~~access~~ data,* **[Doing discloses a "storage control portion" (FIG. 2, element 221) which is included on every CPU. See paragraph [0116]. Doing teaches accessing the disk drive ("secondary storage such as a disk drive") on the basis of block access.]** *a cache memory temporarily storing the block data sent from the second processor,* **[Doing teaches in FIG. 1, elements 106, 107 and 108]** *and a disk interface which connects the ~~second processor~~ cache memory and the plurality of disk drives and sends the block data temporarily stored in the cache memory to the plurality of disk drives;* **[See Doing FIG. 1, elements 111, 112. The second processor connects the disk interface (Storage IOP) to the plurality of disk drives (DASD) through elements 105, 110.]** *wherein the control unit logically partitions the host interface,* **[Doing teaches in FIG. 1, elements 114,115]** *the first processor,* **[e.g. FIG. 1 element 101A, "CPU" See paragraph [0054] for further logical partitioning of individual processors through multithreading]** *the second processor,* **[Doing discloses a "second processor" e.g. in FIG. 1 element 111: "Storage IOP"]** *the cache memory,* **[e.g. FIG. 1 elements 106, 107, 108, L1 and L2]** *the disk interface,* **[FIG. 1 elements 111 and 112. The "Storage IOP" (111 and 112) can be logically partitioned]** *and, the plurality of disk drives,*

[FIG.1, "DASD"] *and causes the partitioned host interface, the partitioned first processor, the partitioned second processor, the partitioned cache memory, the partitioned disk interface, and the partitioned plurality of disk drives to operate as a plurality of virtual storages independently* **[Doing discloses this limitation in paragraph [0065], lines 1-11]**

Doing, however, does not disclose *expressly "cache memory temporarily storing the block data sent from the second processor"*.

DeKoning *discloses* in column 9, lines 22-24, "The storage processor reads a block of data from a disk in the disk array and stores it to a cache block address in the cache memory region."

Doing and DeKoning are analogous art because they are from the same field of endeavor, that being computer architecture resource management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the storage processor cache into the storage apparatus for partitioning resources to arrive at claims 1, 16, and 18.

The motivation for doing so would have been obvious because systems employ cache memories for temporary data storage that can be accessed quickly.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention having the teachings of DeKoning and Doing before him/her to combine Doing and DeKoning for the benefit of having a system that can efficiently store block data sent from a second processor to obtain the invention as specified in claims 1, 16 and 18.

With respect to **claim 2, and independent claim 18**,

"A storage according to claim 1, wherein the control unit further includes a plurality of cache memories, **[FIG. 1, elements 106, 107, 108]** *and the plurality of cache memories is logically partitioned and allocated to the respective plurality of virtual storages"* **[is disclosed in paragraphs [0053] and [0065] and FIG. 1 and 2] [FIG. 1 teaches the implementation of the control unit (multiple processors) and FIG. 2 teaches the implementation of a plurality of cache memories. Since Doing is partitioning the plurality of processors, the plurality of cache memories are also logically partitioned and allocated to the respective plurality virtual storages.]**

With respect to **claims 4, 6, and 7**,

"A storage according to claim 2, wherein the first processor executes a first hypervisor which performs logical partitioning of the host interface and the first processor **[is disclosed in paragraphs [0035] and [0036] and FIG. 1]** *and wherein the second processor executes a second hypervisor which performs logical partitioning of the plurality of cache memories, the disk interface, the plurality of disk devices and the second processor"* **[is disclosed in paragraphs [0029] and [0036] and FIG. 1]**

With respect to **claim 5, and independent claim 18**,

"A storage according to claim 4, wherein the control unit further includes a plurality of memories which are used by the first processor and a plurality of communication units which connect the first processor and the second processor

[is disclosed in FIG. 1 and paragraph [0053]] *wherein the plurality of memories are logically partitioned by the first hypervisor* **[Doing discloses in paragraph [0138], "The ability of code in hypervisor state to alter the information in configuration register 910 means that the logical partitioning of a system can be dynamically changed. E.g., processors and other resources can be re-allocated to different logical partitions..." Also see paragraph [0065]]** *and the plurality of communication units are logically partitioned by the second hypervisor* **[is disclosed in paragraphs [0035] and [0036]]**

With respect to **claims 8, 11, and 16**,

"A storage according to claim 2 further connected to a supervising terminal, **[FIG. 1, "workstation" elements 114, 115]** *wherein the control unit performs the logical partitioning on the basis of information inputted from the supervising terminal"* **[is disclosed in paragraphs [0042] and [0046]. See FIG. 6]**

With respect to **claims 9 and 12**,

"A storage according to claim 8, wherein, if information to be inputted to the supervising terminal is information to the effect that a host system using the storage emphasizes data transfer rate, an amount of allocation of the plurality of cache memories to a virtual storage to be used by the host system among the plural virtual storages is increased" **[is disclosed in paragraph [0084], FIGs. 1-3, and 7]**

With respect to **claim 10**,

> *"A storage according to claim 8, wherein, if information to be inputted to the supervising terminal is information to the effect that a host system using the storage performs random access in a large area, an amount of allocation of the plurality of cache memories to a virtual storage to be used by the host system among the plural virtual storages is reduced"* **[is disclosed in paragraph [0084], FIGs 1-3, and 7] [Doing teaches, the instruction (from a supervising terminal) has an importance in response time (Where L11-cache cannot respond (i.e., the requested instruction is not in L11-cache), a longer path via cache fill bus 233 through memory management unit 222 must be taken), then reduce the amount of allocation of shared cache to a virtual partition. Doing teaches that an allocation of cache is reduced for a particular partition (processor) when another processor is utilizing it.]**

Note: As applicant alleges on page 15 of the instant remarks, the amendments to claims 13-15 do *not* narrow their scope. Accordingly, the previous rejection should stand by itself. However, should it be found that such amendments do in fact narrow the scope, the limitations are shown in paragraphs [0138] and [0065].

With respect to **claim 13,**

> *"A storage according to claim 8, wherein, if information to be inputted to the supervising terminal is information to the effect that a host system using the storage requires access to a smaller number of large files than that for which processor support to one of the virtual storages is currently set for the host*

system, an amount of allocation of the first processor to the virtual storage to be used by the host system is reduced, and an amount of allocation of the second processor to the virtual storage is increased." **[Armstrong teaches amount of allocation of the first processor to the a virtual storage to be used by the host system among the plural virtual storages is reduced, and an amount of allocation of the second processor to the virtual storage is increased (...each logical partition is allocated one or more processors 12, as well as a portion of the available memory space for use in virtual memory 60. Logical partitions can share specific hardware resources such as processors, such that a given processor is utilized by more than one logical partition.)]**

With respect to **claim 14,**

"A storage according to claim 8, wherein, if information to be inputted to the supervising terminal is information to the effect that a host system using the storage requires access to a larger number of small files than that for which processor support to one of the virtual storages is currently set for the host system, an amount of allocation of the first processor to the virtual storage to be used by the host system is increased, and an amount of allocation of the second processor to the virtual storage is reduced" **[is disclosed in Armstrong et at., column 4, lines 35-67(U.S. Pat. no. 6,279,046, incorporated by reference by Doing and hereafter referred to as Armstrong)] [Armstrong teaches amount of allocation of the first processor to the a virtual storage to be used by the host system among the plural virtual storages is increased, and an amount**

of allocation of the second processor to the virtual storage is reduced (...each logical partition is allocated one or more processors 12, as well as a portion of the available memory space for use in virtual memory 60. Logical partitions can share specific hardware resources such as processors, such that a given processor is utilized by more than one logical partition.)]

With respect to **claim 15**,

"A storage according to claim 11, wherein if information to be inputted to the supervising terminal is information to the effect that a host system using the storage requires sequential access to **[is disclosed in paragraph [0084]]** *a larger file than that for which communication unit support to one of the virtual storages is currently set for the host system, an amount of logical allocation of the plurality of communication units to the virtual storage to be used by the host system is reduced."* **[is disclosed in Armstrong et at., column 4, lines 47-67(U.S. Pat. no. 6,279,046, incorporated by reference by Doing and hereafter referred to as Armstrong).] [Doing discloses in paragraph [0138], "The ability of code in hypervisor state to alter the information in configuration register 910 means that the logical partitioning of a system can be dynamically changed. E.g., processors and other resources can be re-allocated to different logical partitions..."]**

With respect to **claim 17**,

"A storage system according to claim 16, wherein the information inputted to the supervising terminal is information on characteristics of accesses of a computer using the storage, **[Doing discloses in paragraph [0138], "The ability of code in hypervisor state to alter the information in configuration register 910 means that the logical partitioning of a system can be dynamically changed. E.g., processors and other resources can be re-allocated to different logical partitions..."]** *and the storage calculates an amount of logical partitioning of resources provided in the storage on the basis of the information on characteristics of accesses inputted to the supervising terminal, and performs the logical partitioning using a result of the calculation."* **[disclosed in paragraphs [0040] and [0042]] [Doing teaches the inputted information to the supervising terminal (via operating system software) has characteristics of accesses of a computer using the storage (running in hypervisor state). The storage (NAS or system) calculates an amount of logical partitioning of resources provided in the storage (configuration information) on the basis of the inputted information and performs the logical partitioning using the result of the calculation (dynamically re-allocate resources to logical partitions).]**

Response to Amendment

Applicant's arguments filed **May 10, 2006** have been fully considered but they are not deemed to be persuasive and, as required by **M.P.E.P. 707.07(f)**, a response to these arguments appears below.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

1ST POINT OF ARGUMENT:

With respect to the arguments on page 12, lines 20-21 of the applicant's remarks, the examiner believes that Doing teaches partitioning of the disk interface. The examiner cites FIG. 1, elements 105, 111, and 112. These elements teach partitioning of the disk interface (bus interface) into (at least two) different subsets of storage processor-and storage resources, e.g.

2ND POINT OF ARGUMENT:

With respect to the argument on page 13, lines 1-4 of the applicant's remarks, please refer to the secondary reference DeKoning et al. (U.S. Patent Number 6,216,199).

3rd POINT OF ARGUMENT:

With respect to the argument on page 13, lines 15 through page 14, lines 1-2 of the applicant's remarks, Doing discloses a first processor (FIG. 1, element 101A) and a second processor (FIG. 1, element 111) that anticipate the applicant's claimed limitations. See paragraph [0065], lines 1-11.

CONCLUSION

Direction of Future Correspondences

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status

information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Reginald G. Bragdon

Horace L. Flournoy

Reginald G. Bragdon

Patent Examiner
Art unit: 2189

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